

STOCHASTIC NETWORK CALCULUS FOR END-TO-END DELAY EVALUATION OF AVIONICS MULTI-HOP VIRTUAL LINKS

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Abstract:

The VL (Virtual Link) concept used by AFDX network of modern aircraft such as A380 represents a big assumption for input flows characteristics. But mapping of many VL on a multi switch Ethernet architecture lead to potential congestion on a port of a (given) switch. Thus, there is strong need to prove that no frame will be lost by the network (no switch queue will overflow) and to evaluate the end-to-end transfer delay through the network. Several approaches have been proposed for this evaluation. Deterministic network calculus gives a guaranteed upper bound on end-to-end delays, while simulation produces more accurate results on a given set of scenarios. Stochastic network Calculus has been successfully used to calculate end-to-end delays distribution of mono switch flows. In this paper, we show how it can be extended to multi switches flows.

Keywords: Network calculus, end-to-end- delay, AFDX, stochastic

1. INTRODUCTION

The evolution of avionics embedded systems and the amplification of the integrated functions number in the current aircraft imply a huge increase in the exchanged data quantity and thus in the number of connections between functions. Consequently, the growth of the number of multi point communication, such as the development of embedded networks, constitutes one of the major stakes of new generation architectures.

The solution adopted by Airbus for the new A 380 generation consists in the utilization of a recognized standard which allows a re-use of development tools as well as of existing communication components while achieving better performance. It consists of the Switched Ethernet technology which benefits from a long industrial use *IEEE 802.1D, Local and Metropolitan Area Network: Media Access Control Level Bridging*. (1998), that allows to have confidence in the reliability of the material and on the facility

of its maintenance. Hence aeronautical systems can integrate of a much more powerful technology than the traditional avionics bus (Switched Ethernet / 100 Mbps).

AFDX (Avionics Full Duplex Switched Ethernet) *ARINC 664, Aircraft Data Network, Part 1: Systems Concepts and Overview*. (2002), *ARINC 664, Aircraft Data Network, Part 2: Ethernet Physical and Data Link Layer Specification*. (2002) and *ARINC 664, Aircraft Data Network, Part 7: Deterministic Networks*. (2003) is a static switched Ethernet network (802.1D tables are statically set up and no spanning tree mechanism is implemented) for determinism purpose. The full duplex switched Ethernet technology guarantees that there are no collisions on the physical links, compared with a vintage Ethernet solution Jasperneite *et al.* (2002). So, it eliminates the inherent indeterminism of vintage Ethernet and the collision frame loss. But, it shifts in fact the problem to the switch level where various flows will enter in competition for the use of

the resources of the switches. This can lead to temporary congestion on an output port of a switch, if at a given time, too much traffic moves towards this port. This can increase significantly end-to-end delays of frames and can even lead to frame losses by overflow of queues.

Flows on an AFDX network are statically identified in order to obtain a predictable deterministic behavior of the application on the network architecture. The analysis of end-to-end delays of frames is necessary in order to characterize the behavior of the application. This analysis has to evaluate, on the one hand an upper bound on the end to end delay of a given flow and on the other hand the distribution of this end-to-end delay. The first one is mandatory for certification reasons, while the second one can help greatly to evaluate the pessimism of the upper bound and is valuable when prototyping the whole system. In this paper, we consider that there is no frame loss (queues are large enough) and we study end-to-end delays distribution of frames. Preliminary results have been presented in Charara *et al.* (2006a), considering a simulation approach. In this paper, we consider a stochastic network calculus approach.

Section 2 specifies the end-to-end delays analysis problem in the context of this paper. Section 3 presents the stochastic network calculus approach for a mono switch and its application to multi switches. Section 4 gives some results and evaluate their pessimism. Section 5 summarizes the paper and gives some guidelines for future works.

2. SCOPE OF THE STUDY

In this Section, we first give a brief overview of the AFDX network. Then, we formulate the problem of end-to-end delay analysis and the way it is addressed in the remaining of the paper.

2.1 The AFDX network

An example of an AFDX network architecture is depicted in Figure 1. It corresponds to a test configuration provided by Airbus for an industrial research study Charara *et al.* (2006b). It is composed of several interconnected switches. There are no buffers on input ports and one FIFO buffer for each output port. The inputs and outputs of the networks are called *End Systems* (the little circles on Figure 1). Each End System is connected to exactly one switch port and each switch port is connected to at most one End System. Links between switches are all full duplex. In Figure 1, values on input and output end systems indicate numbers of application traffic flows. For instance, there are 113 different application traffic flows that are directly transmitted from an end system to switch S1.

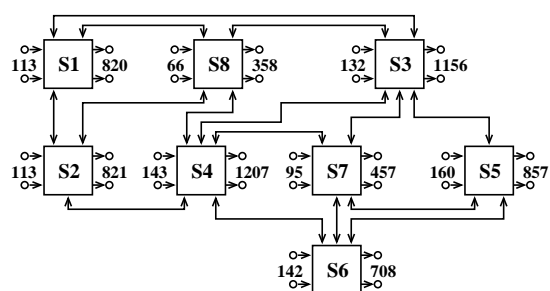


Fig. 1. AFDX network architecture

The end-to-end traffic characterization is done by the definition of Virtual Links. As defined by ARINC-664, Virtual Link (VL) is a concept of virtual communication channels; it has the advantage of statically defining the flows which enter the network *ARINC 664, Aircraft Data Network, Part 7: Deterministic Networks.* (2003).

End Systems exchange Ethernet frames through VL. Switching a frame from a transmitting to a receiving End System is based on a VL (deterministic routing). The Virtual Link defines a logical unidirectional connection from one source End System to one or more destination End Systems. It is a path with multicast characteristic. The routing of each VL is statically defined by the designer. He arbitrarily chooses one path between the source and end destination for the VL. One possible criterion is the load balancing between links. Only one End System within the Avionics network can be the source of one Virtual Link, (i.e., Mono Transmitter assumption).

Traffic on each Virtual Link is sporadic. Most of the time, physical links of an AFDX network are lightly loaded. As an example, on the configuration of Figure 1, most of the links are loaded at less than 15 % and no link is loaded at more than 21 % (see Charara *et al.* (2006b) for details). However, a congestion can occur at any time at any output port in case of a transient burst of traffic. This lead to variable end-to-end delays for frames of a given VL. Bursts of traffic occur when frames of different VLs reach the same output port at the same time. This event is closely related to the emission of the frames of the different VLs, i.e. the phasing between VLs.

2.2 Scope of the end-to-end delay analysis

Frames exchanged between End Systems have to respect temporal constraints. So, the end-to-end delay of each path of each VL has to be studied. It includes the following characteristics :

- The upper bound for the end-to-end delay, which corresponds to the longest aggregate waiting service time for the frame in queues. Studies have been done in order to evaluate this upper bound. Deterministic Network Calculus approach Cruz (1991a) and Cruz (1991b) gives the

latency upper bound of any elementary network entity. Then, guaranteed upper bounds on end-to-end delays can be derived Frances *et al.* (2006) and Le Boudec (1998). Most of the time, those bounds cannot be reached as they are based on pessimistic assumptions. An open question is to determine how pessimistic those bounds are. The model checking approach Alur and Dill (1994) and Larsen *et al.* (1997) determines an exact upper bound for the end-to-end delay and the corresponding scenario Charara *et al.* (2006b) and Ermont *et al.* (2006), but it cannot be applied to a realistic network configuration, due to combinatorial explosion. Nevertheless, this approach can help greatly to better understand the behavior of the network.

- The distribution of the end-to-end delay between its lower bound and its upper bound. Simulation is a promising approach to obtain this distribution, provided it covers a representative subset of all possible scenarios. Preliminary results have been presented in Charara *et al.* (2006a). They have been obtained by focussing the simulation on the relevant part of the network configuration, using a taxonomy of VLs. However, simulation can't cope with too large network configurations, due to their huge number of possible scenarios.

In this paper, we propose a stochastic network calculus approach in order to obtain a distribution of end-to-end delays. Such an approach could deal with arbitrarily large network configurations. The next section presents the stochastic network calculus approach.

3. STOCHASTIC NETWORK CALCULUS ANALYSIS

The objective of these works is to obtain the distribution of end-to-end delay for a given path of a VL. The stochastic network calculus, applied to mono switch flows, has already presented in Ridouard *et al.* (2007). But we detail again this approach in section 3.1. Then, we describe the method to obtain the distribution of end-to-end delay for a given path of a VL crossing several switches.

3.1 End-to-end delay for a given mono hop path of a VL

In this section, we are only interested about mono switch. We, first, explain why stochastic network calculus theory can be applied in the AFDX context. Then we show how we apply stochastic network calculus results to our context.

3.1.1. *Applicability of the analysis* In the present study, the AFDX networks considered, have only a

single FIFO buffer for each switch output port. Consequently, all the flows (VLs) have the same priority and each switch output port can be considered as servicing an aggregate traffic (all the VLs crossing this port) with a constant rate c which is the capacity of the output link (e.g. $100Mbps$). Moreover, the individual flows are shaped separately at network access, by the assumption of the minimum delay between the emission of two consecutive frames, i.e. BAG (Bandwidth Allocation Gap). It corresponds to a network considering *EF PHB* (Expedited Forwarding Per-Hop Behavior) service of *DiffServ* (Differentiated Services) architecture Davie *et al.* (2002). The nodes (i.e. the switch output ports) are said *PSRG* (Packet Scale Rate Guarantee) nodes Bennett *et al.* (2002) and the *EF* traffic at a node is served with a rate independently of any other traffic transiting the same node. The stochastic network calculus approach presented in Vojnović and Le Boudec (2002) applies to such network configurations.

More formally, a node is *PSRG* (c, e) for a flow means this flow is guaranteed a rate c , with a latency (error term) e . Therefore if we denote d_n , the departure of the n^{th} packet of the *EF* aggregate flow, in order of arrivals, d_n satisfies

$$d_n \leq f_n + e$$

where f_n is calculated recursively as $f_0 = 0$ and

$$f_n = \max \{a_n, \min\{d_{n-1}, f_{n-1}\}\} + \frac{l_n}{c}, n \geq 1$$

where the n^{th} packet arrives at time a_n with l_n bits.

The error term e is the extra waiting time due to non *EF* traffic. In our context, there is only *EF* traffic crossing each switch output port. Consequently, we have $e = 0$.

The end-to-end delay of a given path of a VL is the sum of the delays in each switch crossed by the path. The delay in a switch is composed of the switching delay (filtering and forwarding operations), the waiting time in the output buffer and the transmission time on the output link. The switching delay is a constant that depends on the switch technology ($16 \mu s$ for switches used by Airbus). The transmission time is a function of the link rate (typically $100 Mbps$). The waiting time of a frame depends on the load of the output port (backlog) at the arrival time of the frame. Therefore, the end-to-end delay is not constant due to the waiting times in the switch output ports it crosses.

The works presented by Vojnović and Le Boudec in Vojnović and Le Boudec (2002) and Vojnović and Le Boudec (2003) about networks with *EF PHB* service can be used to calculate the distribution of this waiting time for each switch. It is based on the probability of bound buffer overflow in the switch output port. Such a problem was previously addressed in Chang

et al. (2001) and Kesidis and Kostantopoulos (2000). Results presented in Vojnović and Le Boudec (2002) and Vojnović and Le Boudec (2003) have proposed the tightest upper bounds.

Vojnović and Le Boudec make the four assumptions presented in appendix A. The assumption (A1) imposes to define a service curve for nodes. But a property of PSRG is that a PSRG $(c, 0)$ implies the service curve $\beta(t) = ct$. Consequently, the property (A1) is respected. As VLs are independent at network access, assumption (A2) is respected. Concerning assumption (A3), in the AFDX context, each VL is regulated by a leaky-bucket $(\alpha_i(t) = \rho_i t + \sigma_i)$ defined in the following way. σ_i is the maximum length of a frame of the VL, denoted S_{max} . ρ_i is the VL maximum flow, $\frac{S_{max}}{BAG}$, where BAG is the minimum delay between the emission of two consecutive frames of the VL by its source end system. Therefore assumption (A4) is valid with $\xi_i = \rho_i$.

Vojnović and Le Boudec define the concept of EF traffic inputs homogeneously regulated (see appendix A). In our context, traffic inputs are homogeneously regulated when all VLs have the same S_{max} and BAG and they are heterogeneously regulated otherwise.

In the following, we consider only homogeneous traffic inputs.

As all the assumptions made by Vojnović and Le Boudec are respected, their results can be applied in our context.

3.1.2. Application of the analysis In Vojnović and Le Boudec (2003) the tightest backlog bound (given by Theorem 1 of appendix B) for homogeneous regulation of traffic inputs is established.

These definitions of probability (Theorem 1) can be seen as a fraction of time the backlog is above the level b . In order to determine the waiting delay in the output buffer, we need to know the backlog in the buffer at the arrival time of a frame f . It is called the complementary distribution of the backlog. Informally, it is the probability that the size of all frames in the output buffer, including f exceeds the level b . This probability is denoted \mathbb{P}_A and named the Palm probability Baccelli and Bremaud (2000). Vojnović and Le Boudec proved Corollary 1 of Appendix B.

Let $d(0)$ denoted the delay through a node of a frame arriving in the node at time 0. The Theorem 2 of appendix B presents the distribution of delay. $\mathbb{P}(d(0) > u)$ is the probability that $d(0)$ exceeds u .

3.2 End-to-end delay for a given multi hop path of a VL

In this section, we present the method used to obtain the distribution of the end-to-end delay of packet. The

packet crosses a network and follows the path of a VL from source to destination.

Unfortunately, the stochastic Network Calculus analysis is valid only for VL crossing a mono switch Ridouard *et al.* (2007). To apply the stochastic network calculus for a given multi hop path of a VL, a solution is to calculate the delay crossing each switch and finally to sum up the different delays. But a known property for network calculus is the *Pay Bursts Only Once* Le Boudec and Thiran (2001). This property shows that the results obtained are not tighter. Then we cannot extend the first results Ridouard *et al.* (2007) obtained for mono switch, to multi hop path without analysing the propagation of the end-to-end delay. But there exist results for deterministic Network Calculus for VL with multi hop path :

Considering the following assumptions :

- Independent input flows,
- Inputs flows are regulated by leaky buckets,
- Each switch is a FIFO service curve

In Le Boudec and Thiran (2001), the authors demonstrate that if these assumptions are respected, for a given multi hop path of a VL, the switches crossed can be concatenated to an only switch with an arbitrary service curve. And the problem can be transform to an only VL and an only switch. Let VL_1 be a VL crossing n ($n > 0$) switches, $e_S - S_1 \dots S_n - e_q$ and illustrated by the Figure 2. e_S represents the end system source of VL_1 and e_q its end system destination. S_i ($i \in \{1, \dots, n\}$) denotes the output port of the i^{th} switch crossed by VL_1 .

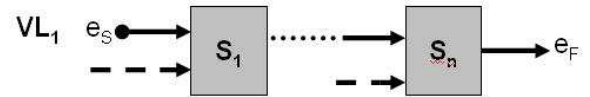


Fig. 2. VL_1 , the VL crossing two switches

In Le Boudec and Thiran (2001), it has been proved that the arrival curves of input flows of the same output port can be aggregated. Consequently, without loss of generality, we consider only the case of two flows coming in each output buffer, f_1 , the flow of VL_1 and the flow aggregated of others flows. To determine the delay through a node of a frame, we must determine the service curve to the flow of the frame.

In Le Boudec and Thiran (2001), the authors prove that if $\beta_i(t) = Rt + T$ be the service curve of a node S_i and if each node S_i ($1 \leq i \leq n$) serves two flows f_1 and f_2 (the flow f_i ($i = 1, 2$) has an arrival curve $\alpha_i(t) = \rho_i t + \sigma_i$. If $\rho_1 + \rho_2 < R$), then for S_i , the flow f_1 has a service curve equals to $\beta_i^{f_1}(t) = (R - \rho_2)t + T + \frac{\sigma_2}{R}$. Moreover, at the output, the flow f_1 has the arrival curve $\alpha_1^*(t) = \rho_1 t + \sigma_1 + \rho_1(T + \frac{\sigma_2}{R})$.

Then, for the flow f_1 , we can determine the arrival curve and the service curve for each node S_i ($1 \leq i \leq n$) and all the nodes of the path can be reduce to an

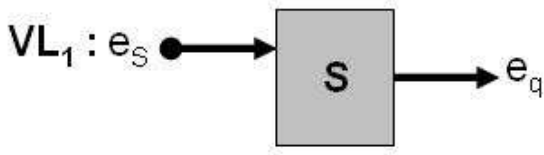


Fig. 3. The node created for VL_1

only node, as illustrated by the Figure 3. For the flow f_1 , the node created, has the following service curve :

$$\beta^{f_1} = \beta_1^{f_1} \otimes \beta_2^{f_1} \otimes \dots \otimes \beta_n^{f_1}$$

Where $\beta_i^{f_1}$ is the service curve of the flow f_1 for the node S_i

And \otimes , the min-plus convolution given by :
 $(f \otimes g)(t) = \inf_{0 \leq s \leq t} \{f(s) + g(t - s)\}$.

But for the flow f_1 , the node created has a service curve β^{f_1} , with the form $\beta^{f_1}(t) = Rt + T$ where R is the rate to serve f_1 and T , the waiting time before serve. To apply the works presented in Section 3.1, the service curve must be super-additive (i.e. $\beta(t + s) \geq \beta(t) + \beta(s)$) and then $T \leq 0$. But T is a waiting time ($T > 0$) and the service curve β^{f_1} is not super-additive. We can resolve this problem : we use the following service curve: $\beta^{f_1}(t) = Rt$ to compute the end-to-end delay. T is summed up to the final worst case end-to-end delays, since T is a waiting time summed up to the final worst case end-to-end delays.

We are assumed that flows are homogeneous. But since for each VL we just consider one switch and one flow (the given VL), we can erase this assumption for the following of our works.

Using the works developed for the deterministic network calculus Le Boudec and Thiran (2001), we can apply the stochastic network calculus (presented in Section 3.1) since the problem is transformed to a mono hop path.

4. RESULTS ON TWO HOP VL

In this section, the stochastic Network Calculus analysis presented in the previous section, is applied to AFDX network configurations. The network configuration is composed of three switches, five paths of VL and six end systems. It is depicted by the Figure 4.

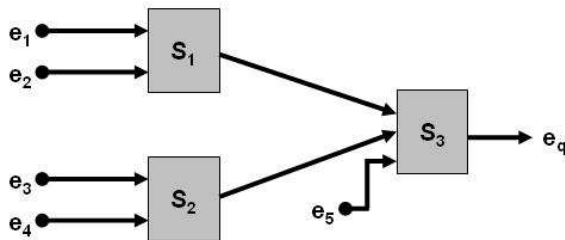


Fig. 4. The network configuration

Each switch output port serves the aggregate traffic (all the VLs crossing this port) with a constant rate

	C_1	C_2	C_3	C_4	C_5	C_6
r	1	2	3	4	5	6
load of S_3	5 %	10 %	15 %	20 %	25 %	30 %

Table 1. Network configurations

	Simulation	Stoc. NC
C_1	237	241
C_2	300	487
C_3	310	740
C_4	372	1000
C_5	394	1269
C_6	399	1543

Table 2. Upper bounds of end-to-end delay

$c = 100b/\mu s$ (see section 3.1.1). Each path supports the same number of VL and all VLs of the network configuration have the same end system destination, e_q . In our context, traffic inputs are homogeneously regulated (see section 3.1.1) then, all VLs have the same length S_{max} ($= 4000$ bits) and same BAG ($= 4000\mu s$).

In this section, we study VL crossing two switches. Therefore, we do not calculate the distribution of end-to-end delay of VL with the path $e_5 - S_3 - e_q$. Moreover, VLs are homogeneous and each path has the same number, denoted r , of VLs. Then, in, our context, VLs crossing two switches have the same distribution of end-to-end delay. Consequently, we just calculate the end-to-end delay of the VL, denoted VL_1 , with the path $e_1 - S_1 - S_3 - e_q$.

In the following, the results presented concern the configurations of Table 1.

The Figure 5 presents the distribution of the probability $\mathbb{P}(d(0) > u)$ about the end-to-end delay of vl_1 computed with the stochastic network calculus analysis.

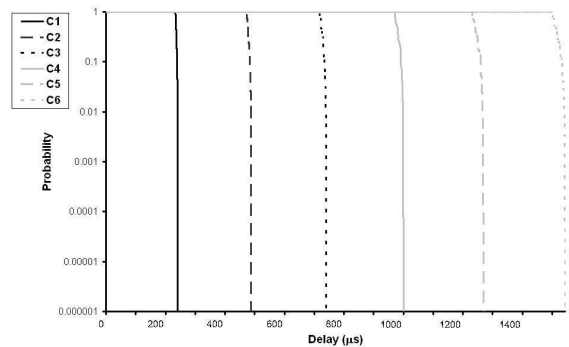


Fig. 5. Distribution of end-to-end delay with Stochastic network calculus

The distribution of delays obtained, have higher values when the load of the network configuration increases. Thus the Delays for configuration C_1 are distributed between 233 and 241, while for the configuration C_6 , delays are mostly distributed between 1499 and 1543 μs .

The Table 2 presents the upper bounds of end-to-end delay obtained by the simulation and by the stochas-

tic network calculus for each network configuration (presented in Table 1. It shows that the difference between the results of simulation and stochastic network calculus increases with the load of the configuration. Consequently, the pessimism of stochastic network calculus approach increases with the load of the network.

Finally, the Figure 6 depicts the comparison between the results obtained with the stochastic network calculus, the simulation, the model checking and the deterministic network calculus for the configuration C_1 . The model checking determines the exact worst-case end-to-end delay since it explores all possible scenarios. The result of the deterministic network calculus is higher than the result of the model checking since it considers a pessimistic upper bound on traffic. The simulation and the stochastic network calculus obtain similar worst-case end-to-end delay than the model checking.

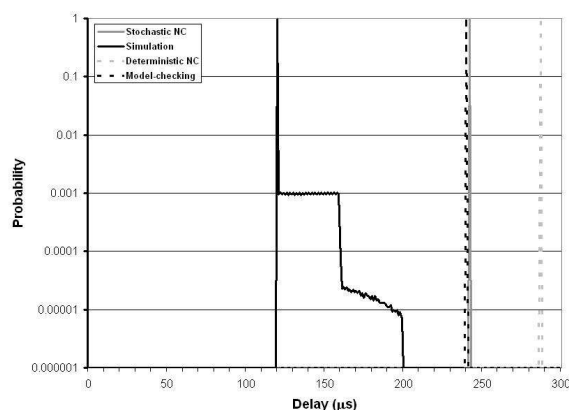


Fig. 6. Comparison of upper bounds of different approaches

5. CONCLUSION

It has been already proved Ridouard *et al.* (2007) that the stochastic network calculus approach can be applied to AFDX context. The results are interesting and this method is complementary to the simulation and the deterministic network calculus. In this paper, we detail the scope of end-to-end delays analysis on an industrial switched Ethernet network for multi switches flows. Two important characteristics are analysed: the upper bound of end-to-end delays and their distribution. The first one is mandatory for certification reasons. The second one can help greatly to evaluate the pessimism of the upper bound and is valuable when prototyping the whole system. We have detailed how we apply the stochastic network calculus for multi switches flows in using the works about the existing for deterministic network calculus.

The obtained distribution of end-to-end delay is pessimistic, compared with the real behavior of the network calculated by the model checking and estimated

by a simulation approach, but much less pessimistic than the upper bound obtained by a deterministic network calculus approach.

The upper bound calculated by the stochastic network calculus is near of real worst-case delay obtained by the model-checking. but we cannot compare with a load more important since it cannot be calculated by model-checking.

In this paper we validate our method for two hop path. We must again validate our results to path with any number of switches.

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Appendix A. DEFINITIONS AND ASSUMPTIONS OF VOJNOVIĆ

- let $A(t) = \sum_{i=1}^{\mathcal{I}} A_i(t)$ be the input aggregate.
- $\alpha(t) = \sum_{i=1}^{\mathcal{I}} \alpha_i(t)$ denotes the aggregate arrival curve.
- $\rho = \sum_{i=1}^{\mathcal{I}} \rho_i$ denotes the upper bound on the aggregate sustainable rate.
- τ is the intersection between the aggregate arrival curve α and the service curve β :
 $\tau = \inf\{u \geq 0 \mid \alpha(u) \leq \beta(u)\}$.
- Let $Q(t)$ be the backlog at time t of a node.
- let $\tilde{Q}(t)$ be an upper bound of the backlog and $\tilde{Q}(t) = \sup_{t-\tau \leq s \leq t} \{A(t) - A(s) - \beta(t-s)\}$.

Definition 1. The EF traffic inputs are homogeneously regulated, if they are regulated by the same function :

$\alpha_i(t) = \alpha_1(t)$, for all $i \in \{1, \dots, \mathcal{I}\}$. Otherwise, the EF traffic inputs are heterogeneously regulated.

Vojnović and Le Boudec make the following assumptions :

(A1) Nodes offer to the EF aggregate traffic, a service curve β , means that for all t ($t \geq 0$), there exists s , ($s \leq t$) such that

$$A^*(t) \geq A(s) + \beta(t-s)$$

where $A(t)$ denote (*resp.* $A^*(t)$) the input (*resp.* the output) EF aggregate data from the node on the interval $[0, t]$.

(A2) The EF traffic inputs are mutually independent at network ingress points.

Let A_i ($1 \leq i \leq \mathcal{I}$) be the independent EF input traffic.

(A3) Every EF input is regulated at the network ingress point. Consequently, for all i , ($1 \leq i \leq \mathcal{I}$), there exists a wide-sense increasing function α_i (called arrival curve) such that :

$$A_i^0(t) - A_i^0(s) \leq \alpha_i(t-s), \text{ for any } s \leq t$$

where $A_i^0(t)$ represents the data observed on $[0, t]$ of the input traffic A_i at the network ingress.

(A4) $\mathbb{E}[A_i^0(t) - A_i^0(s)] \leq \xi_i(t-s)$, for any $s \leq t$ where $\xi_i = \lim_{t \rightarrow \infty} \frac{\alpha_i(t)}{t}$

Appendix B. RESULTS OF VOJNOVIĆ

Theorem 1. Homogeneous case : Assuming (A1)-(A4) and if $\rho < c$, for any t , the upper bound of the probability (denoted \mathbb{P}) that the backlog is above a given level b is

$$\mathbb{P}(Q(t) > b) \leq \mathbb{P}(\tilde{Q}(t) > b) \leq \sum_{k=0}^{K-1} \exp(-\mathcal{I}g(s_k, s_{k+1})) \quad (\text{B.1})$$

for any $K \in \mathbb{N}$, and any $0 = s_0 \leq s_1 \leq \dots \leq s_K = \tau$. where,

- for, $b > \alpha(v) - \beta(u)$, $g(u, v) = +\infty$
- for, $b < \rho v - \beta(u)$, $g(u, v) = 0$
- else,

$$g(u, v) = \frac{\beta(u)+b}{\alpha(v)} \ln \frac{\beta(u)+b}{\rho v} + \left(1 - \frac{\beta(u)+b}{\alpha(v)}\right) \ln \frac{\alpha(v)-\beta(u)-b}{\alpha(v)-\rho v}$$

Corollary 1. Let a node that offers a service curve $\beta(t) = ct$ and A denote the input aggregate with stationary increments and intensity ρ ($\rho < c$). Then, if a packet arrives in the node at time 0, it holds,

$$\mathbb{P}_A(Q(0) > b) \leq \frac{c}{\rho} \mathbb{P}(\tilde{Q}(0) > b) \quad (\text{B.2})$$

Theorem 2. For a PSRG($c, 0$) node and for $u \geq 0$, it is established that, if a node arrives in node at time 0,

$$\begin{aligned} \mathbb{P}(d(0) > u) &\leq \mathbb{P}_A(Q(0) > cu) \\ &\leq \frac{c}{\rho} \mathbb{P}(\tilde{Q}(0) > cu) \end{aligned} \quad (\text{B.3})$$