Stochastic network calculus for end-to-end delays distribution evaluation on an avionics switched Ethernet

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Abstract

AFDX (Avionics Full Duplex Switched Ethernet, ARINC 664) used for modern aircraft such as Airbus A380 represents a major upgrade in both bandwidth and capability for aircraft data networks. Its reliance on Ethernet technology helps to lower some of the implementation costs, though the requirement for guaranteed service does present challenges to system designers.

Thus, the problem is to prove that no frame will be lost by the network (no switch queue will overflow) and to evaluate the end-to-end transfer delay through the network.

Several approaches have been proposed for this evaluation. Deterministic network calculus gives a guaranteed upper bound on end-to-end delays, while simulation produces more accurate results on a given set of scenarios. In this paper, we propose a stochastic network calculus approach in order to evaluate the distribution of end-to-end delays. We evaluate the pessimism of the results on some typical AFDX flows, as described by Virtual Links.

1. Introduction

The evolution of avionics embedded systems and the amplification of the integrated functions number in the current aircraft imply a huge increase in the exchanged data quantity and thus in the number of connections between functions. Consequently, the growth of the number of multi point communication, such as the development of embedded networks, constitutes one of the major stakes of new generation architectures.

The solution adopted by Airbus for the new A 380 generation consists in the utilization of a recognized standard which allows a re-use of development tools as well as of existing communication components while achieving better performance. It consists of the Switched Ethernet technology which benefits from a long industrial use [1], that allows to have confidence in the reliability of the material and on the facility of its maintenance. Hence aeronautical systems can integrate of a much more powerful technology than the traditional avionics bus (Switched Ethernet / 100 Mbps).

AFDX (Avionics Full Duplex Switched Ethernet) [2, 3, 4] is a static switched Ethernet network (802.1D tables are statically set up and no spanning tree mechanism is implemented) for determinism purpose. The full duplex switched Ethernet technology guarantees that there are no collisions on the physical links, compared with a vintage Ethernet solution [16]. So, it eliminates the inherent indeterminism of vintage Ethernet and the collision frame loss. But, it shifts in fact the problem to the switch level where various flows will enter in competition for the use of the resources of the switches. This can lead to temporary congestion on an output port of a switch, if at a given time, too much traffic moves towards this port. This can increase significantly end-to-end delays of frames and can even lead to frame losses by overflow of queues.

Flows on an AFDX network are statically identified in order to obtain a predictable deterministic behavior of the application on the network architecture. The analysis of end-to-end delays of frames is necessary in order to characterize the behavior of the application. This analysis has to evaluate, on the one hand an upper bound on the end to end delay of a given flow, on the other hand the distribution of this end-to-end delay. The first one is mandatory for certification reasons, while the second one can help greatly to evaluate the pessimism of the upper bound and is valuable when prototyping the whole system. In this paper, we consider that there is no frame loss (queues are large enough) and we study end-to-end delays distribution of frames. Preliminary results have been presented in [10], considering a simulation approach. In this paper, we consider a stochastic network calculus approach.

Section 2 specifies the end-to-end delays analysis problem in the context of this paper. Section 3 presents the stochastic network calculus approach. Section 4 gives some results and evaluate their pessimism. Section 5 summarizes the paper and gives some guidelines for future works.

2. Scope of the study

In this section, we first give a brief overview of the AFDX network. Then, we formulate the problem of end-to-end delay analysis and the way it is addressed in the remaining of the paper.

2.1. The AFDX network

An example of an AFDX network architecture is depicted Figure 1. It corresponds to a test configuration provided by Airbus for an industrial research study [9]. It is composed of several interconnected switches. There are no buffers on input ports and one FIFO buffer for each output port. The inputs and outputs of the networks are called *End Systems* (the little circles on Figure 1). Each End System is connected to exactly one switch port and each switch port is connected to at most one End System. Links between switches are all full duplex. In Figure 1, values on input and output end systems indicate numbers of application traffic flows. For instance, there are 113 different application traffic flows that are directly transmitted from an end system to switch $S1$.

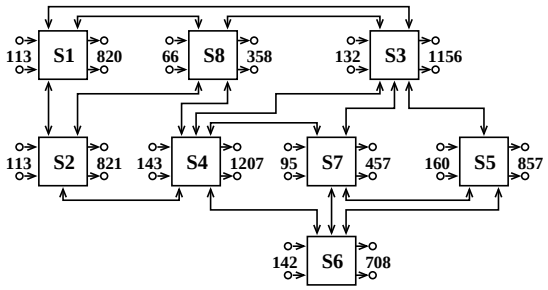

Figure 1. AFDX network architecture

The end-to-end traffic characterization is done by the definition of Virtual Links. As defined by ARINC-664, Virtual Link (VL) is a concept of virtual communication channels; it has the advantage of statically defining the flows which enter the network [4].

End Systems exchange Ethernet frames through VL. Switching a frame from a transmitting to a receiving End System is based on a VL (deterministic routing). The Virtual Link defines a logical unidirectional connection from one source End System to one or more destination End Systems. It is a path with multicast characteristic. The routing of each VL is statically defined by the designer. He arbitrarily chooses one path between the source and end destination fo the VL. One possible criterion is the load balancing between links. Only one End System within the Avionics network can be the source of one Virtual Link, (i.e., Mono Transmitter assumption).

Traffic on each Virtual Link is sporadic. Most of the time, physical links of an AFDX network are lightly loaded. As an example, on the configuration of Figure 1, most of the links are loaded at less than 15 % and no link is loaded at more than 21 % (see [9] for details). However, a congestion can occur at any time at any output port in case of a transient burst of traffic. This lead to variable end-to-end delays for frames of a given VL. Bursts of traffic occur when frames of different VLs reach the same output port at the same time. This event is closely related to the emission of the frames of the different VLs, i.e. the phasing between VLs.

2.2. Scope of the end-to-end delay analysis

Frames exchanged between End Systems have to respect temporal constraints. So, the end-to-end delay of each path of each VL has to be studied. It includes the following characteristics :

- The upper bound for the end-to-end delay, which corresponds to the longest aggregate waiting service time for the frame in queues. Studies have been done in order to evaluate this upper bound. Deterministic Network Calculus approach [11, 12] gives the latency upper bound of any elementary network entity. Then, guaranteed upper bounds on end-to-end delays can be derived [15, 19]. Most of the time, those bounds cannot be reached as they are based on pessimistic assumptions. An open question is to determine how pessimistic those bounds are. The model checking approach [5, 18] determines an exact upper bound for the end-to-end delay and the corresponding scenario [9, 14], but it cannot be applied to a realistic network configuration, due to combinatorial explosion. Nevertheless, this approach can help greatly to better understand the behavior of the network.

- The distribution of the end-to-end delay between its lower bound and its upper bound. Simulation is a promising approach to obtain this distribution, provided it covers a representative subset of all possible scenarios. Preliminary results have been presented in [10]. They have been obtained by focussing the simulation on the relevant part of the network configuration, using a taxonomy of VLs. However, simulation can't cope with too large network configurations, due to their huge number of possible scenarios.

In this paper, we propose a stochastic network calculus approach in order to obtain a distribution of end-to-end delays. Such an approach could deal with arbitrarily large network configurations. The next section presents the stochastic network calculus approach.

3. Stochastic network calculus analysis

First, we explain why stochastic network calculus theory can be applied in the AFDX context. Then we show how we apply stochastic network calculus results to our context.

3.1. Applicability of the analysis

As mentioned earlier, the aim is to obtain the distribution of end-to-end delay for a given path of a VL. The

AFDX networks considered in the present study have a single FIFO buffer for each switch output port. That means that flows (VLs) all have the same priority. Consequently, each switch output port can be considered as servicing an aggregate traffic (all the VLs crossing this port) with a constant rate c which is the capacity of the output link (e.g. 100 Mbps). Moreover, the individual flows are shaped separately at network access, by the assumption of the minimum delay between the emission of two consecutive frames, i.e. BAG (Bandwidth Allocation Gap). It corresponds to a network considering *EF PHB* (Expedited Forwarding Per-Hop Behavior) service of *DiffServ* (Differentiated Services) architecture [13]. The nodes (i.e. the switch output ports) are said *PSRG* (Packet Scale Rate Guarantee) nodes [7] and the *EF* traffic at a node is served with a rate independently of any other traffic transiting the same node. The stochastic network calculus approach presented in [20] applies to such network configurations.

More formally, a node is *PSRG* (c,e) for a flow means this flow is guaranteed a rate c, with a latency (error term) e. Therefore if we denote d_n, the departure of the n^{th} packet of the *EF* aggregate flow, in order of arrivals, d_n satisfies

$$d_n \leq f_n + e$$

where f_n is calculated recursively as $f_0 = 0$ and

$$f_n = \max\{a_n, \min\{d_{n-1}, f_{n-1}\}\} + \frac{l_n}{c},\ n \geq 1$$

where the n^{th} packet arrives at time a_n with l_n bits.

The error term e is the extra waiting time due to non *EF* traffic. In our context, there is only *EF* traffic crossing each switch output port. Consequently, we have $e = 0$.

The end-to-end delay of a given path of a VL is the sum of the delays in each switch crossed by the path. The delay in a switch is composed of the switching delay (filtering and forwarding operations), the waiting time in the output buffer and the transmission time on the output link. The switching delay is a constant that depends on the switch technology (16 μs for switches used by Airbus). The transmission time is a function of the link rate (typically 100 Mbps). The waiting time of a frame depends on the load of the output port (backlog) at the arrival time of the frame. Therefore, the end-to-end delay is not constant due to the waiting times in the switch output ports it crosses.

The works presented by *Vojnović* and *Le Boudec* in [20, 21] about networks with *EF PHB* service can be used to calculate the distribution of this waiting time for each switch. It is based on the probability of bound buffer overflow in the switch output port. Such a problem was previously addressed in [8, 17]. Results presented in [20, 21] have proposed the tightest upper bounds.

Vojnović and *Le Boudec* make the four assumptions presented in appendix A. The assumption (A1) imposes to define a service curve for nodes. But a property of *PSRG* is that a PSRG $(c, 0)$ implies the service curve $\beta(t) = ct$. Consequently, the property (A1) is respected. As VLs are independent at network access, assumption (A2) is respected. Concerning assumption (A3), in the AFDX context, each VL is regulated by a leaky-bucket ($\alpha_i(t) = \rho_i t + \sigma_i$) defined in the following way. σ_i is the maximum length of a frame of the VL, denoted S_{max}. ρ_i is the VL maximum flow, $\frac{S_{max}}{BAG}$, where BAG is the minimum delay between the emission of two consecutive frames of the VL by its source end system. Therefore assumption (A4) is valid with $\xi_i = \rho_i$.

Vojnović and *Le Boudec* define the concept of *EF* traffic inputs homogeneously regulated (see appendix A). In our context, traffic inputs are homogeneously regulated when all VLs have the same S_{max} and BAG and they are heterogeneously regulated otherwise. Results in [20] have been proved for homogeneous and heterogeneous cases, while better results are presented in [21] for homogeneous cases.

As all the assumptions made by *Vojnović* and *Le Boudec* are respected, their results can be applied in our context.

3.2. Application of the analysis

In [20], the tightest backlog bound that holds for homogeneous and heterogeneous regulation of traffic inputs is established. This bound gives the distribution of the backlog and is presented in the theorem 1 of appendix B.

There exists in [21] a tighter bound given by Theorem 2 of appendix B. But this bound holds only for the homogeneous case.

These definitions of probability (Theorem 1 and 2) can be seen as a fraction of time the backlog is above the level b. In order to determine the waiting delay in the output buffer, we need to know the backlog in the buffer at the arrival time of a frame f. It is called the complementary distribution of the backlog. Informally, it is the probability that the size of all frames in the output buffer, including f exceeds the level b. This probability is denoted $\mathbb{P}_A$ and named the Palm probability [6]. *Vojnović* and *Le Boudec* proved corollary 1 of appendix B.

Let $d(0)$ denoted the delay through a node of a frame arriving in the node at time 0. The Theorem 3 of appendix B presents the distribution of delay. $\mathbb{P}(d(0) > u)$ is the probability that $d(0)$ exceeds u.

In order to determine the distribution of the end-to-end delay of a given VL, we first compute

$$\mathbb{P}(d(0) > u)\ with\ u = 0.5, 1.5, 2.5, \ldots$$

until $\mathbb{P}(d(0) > u) = 0$

We have

$$\begin{aligned} \mathbb{P}(d(0) > 0) &= 1\ and \\ \mathbb{P}(d(0) > u) &\geq \mathbb{P}(d(0) > u + 1) \end{aligned}$$

Finally, we consider

$$\mathbb{P}(d(0) = u) = \mathbb{P}(d(0) > u - 0.5) - \mathbb{P}(d(0) > u + 0.5)$$

	S_1	S_2	S_3	S_4	S_5	S_6
r	3	3	3	3	3	3
n_1	5	27	49	71	93	115
n_2	6	32	58	84	110	136
n_3	26	37	48	59	70	81
m_1	4	26	48	70	92	114
m_2	5	31	57	83	109	135
m_3	2	13	24	35	46	57
load	2 %	12 %	22 %	32 %	41 %	51 %

Table 1. studied configurations

4. First results

The stochastic analysis presented in the previous section has been applied to AFDX network configurations. First results are presented in this section. They all concern paths of VL, similar to the vx path of Figure 2.

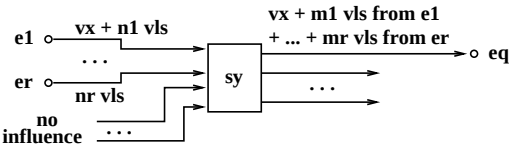

Figure 2. Monoswitch path

v_x is emitted by End System e_1, which emits n_1 other VLs. Among those n_1 VLs, m_1 ones have the same destination End System eq as v_x. Switch sy gets two other kinds of inputs.

The first ones comes from $(r-1)$ End Systems e_2 to e_r. Each of those End Systems emits a given number of VLs (n_i VLs for End System e_i), among which some have e_q as destination End System (m_i VLs for End System e_i).

The other inputs of sy, as well as paths of VLs that do not cross sy have no influence on path $e1 - sy - eq$ of VL vx and can be ignored in the analysis.

It has been shown in [10] that the vx path of Figure 2 corresponds to about 12 % of the paths of a typical industrial AFDX configuration.

Results presented in this paper concern the configurations of table 1.

$S1$ corresponds to a typical VL path of the industrial AFDX configuration of Figure 1. The load of the single switch output port crossed by the VL under study is about 2 %. Configurations $S2$ to $S6$ concerns VLs paths similar to $S1$ with a higher load on the switch output port (between 12 % and 51 %). Since all those configurations contain homogeneous flows, formulas of theorems 1 (V1 approach) and 2 (V2 approach) can be applied. V2 does not apply to the configuration of Figure 1, since flows are not homogeneous.

Figures 3 and 4 present the distributions obtained with the V1 and V2 stochastic network calculus approaches presented in section 3.

With the V1 approach, delays for configuration $S1$ are mostly distributed between 60 and 87 μs. The distribution of delays moves to higher values when the load on the switch output port increases (Delays for configuration $S6$ are mostly distributed between 160 and 250 μs). With the V2 approach, we obtain similar distributions with smaller intervals (between 35 and 48 μs for $S1$, between 50 and 109 μs for $S6$). As expected, the V1 approach is more pessimistic than the V2 one. Remember however that the V2 approach can't apply when flows are heterogeneous.

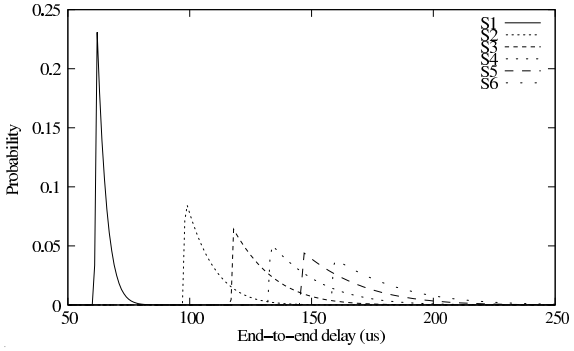

Figure 3. Stochastic network calculus V1

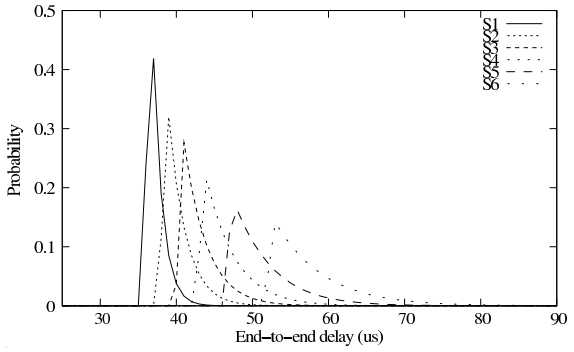

Figure 4. Stochastic network calculus V2

In order to evaluate the relevance of those results we have to state, on the one hand the pessimism of the obtained distribution, on the other hand how far it is from the deterministic upper bound.

We have studied the first point by comparing stochastic network calculus approach results with simulation results obtained with the approach presented in [10]. Figure 5 presents simulation results on $S1$, $S4$ and $S6$.

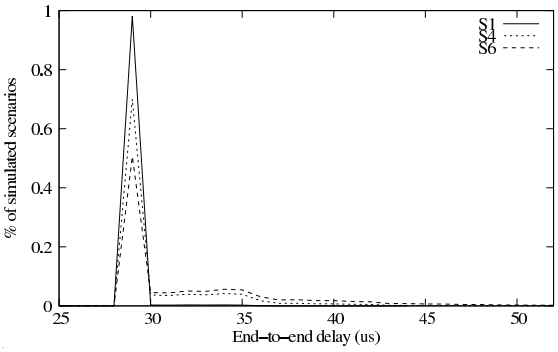

Figure 5. Simulation

It appears that the simulation approach gives significantly smaller end-to-end delays than the stochastic net-

	Simu	St. NC		Det. NC
	$P = 0.9999$	$P = 0.9999$		Det. NC
		V2	V1	
S_1	40	48	87	103
S_2	48	58	167	500
S_3	54	66	213	896
S_4	61	76	250	1293
S_5	69	89	282	1689
S_6	80	106	311	2086

Table 2. Upper bound vs distribution

work calculus approaches. Table 2 gives a rough comparison of the three approaches results.

More precisely, it gives for each network configuration the upper bound that the end-to-end delay will exceed with a probability of 0.0001, considering the simulation approach results and the stochastic network calculus results. We can see that the difference between the simulation and the V1 stochastic approaches increases with the load on the switch output port (40 vs 87 for a load of 2 %, 80 vs 311 for a load of 51 %). It means that the pessimism of the V1 stochastic network calculus approach increases with the load of the switch output port. Conversely, the difference between the simulation and the V2 stochastic approaches evolves in a quite linear way.

In second step, we compared the distribution obtained with the stochastic network calculus approaches with the upper bound obtained by a deterministic network calculus approach. Table 2 gives the upper bound computed for each network configuration (see [9] for details). It shows that the difference between the deterministic upper bound and the stochastic upper bounds that can be exceeded with a probability of 0.0001 increases with the load on the switch output port (106 or 311 vs 2086 for a load of 51 %). It clearly shows that the deterministic approach is much more pessimistic than the stochastic one.

Finally, Figure 6 summarizes results of all the approaches for $S1$ scenario.

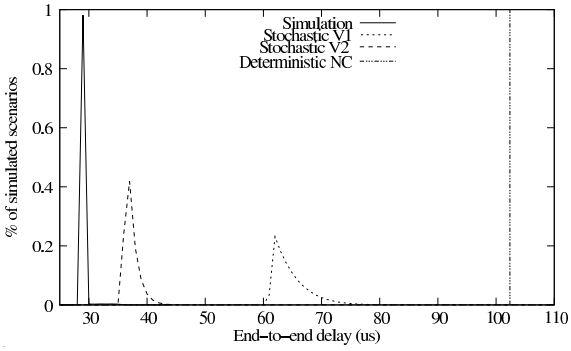

Figure 6. Upper bound vs distribution

5. Conclusion

In this paper, we detail the scope of end-to-end delays analysis on an industrial switched Ethernet network. Two important characteristics are the upper bound of end-to-end delays and their distribution. The first one is mandatory for certification reasons. The second one can help greatly to evaluate the pessimism of the upper bound and is valuable when prototyping the whole system.

Then we present a stochastic network calculus approach that gives an evaluation of the distribution of end-to-end delays of a given flow. The obtained distribution is pessimistic, compared with the real behavior of the network estimated by a simulation approach, but much less pessimistic that the upper bound obtained by a deterministic network calculus approach.

The evaluation presented in this paper only concerns mono-switch flows, which represent about 12 % of a typical industrial network configuration [10]. However, generalization of this approach to multi-switches flows is underway.

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A. Definitions and assumptions of *Vojnović*

- let $A(t) = \sum_{i=1}^{\mathcal{I}} A_i(t)$ be the input aggregate.
- $\alpha(t) = \sum_{i=1}^{\mathcal{I}} \alpha_i(t)$ denotes the aggregate arrival curve.
- $\rho = \sum_{i=1}^{\mathcal{I}} \rho_i$ denotes the upper bound on the aggregate sustainable rate.
- τ is the intersection between the aggregate arrival curve α and the service curve β : $\tau = \inf\{u \geq 0 \mid \alpha(u) \leq \beta(u)\}$.
- Let $Q(t)$ be the backlog at time t of a node.
- let $\tilde{Q}(t)$ be an upper bound of the backlog and $\tilde{Q}(t) = \sup_{t-\tau \leq s \leq t}\{A(t) - A(s) - \beta(t-s)\}$.

Definition 1 *The EF traffic inputs are homogeneously regulated, if they are regulated by the same function : $\alpha_i(t) = \alpha_1(t)$, for all $i \in \{1, \ldots, \mathcal{I}\}$. Otherwise, the EF traffic inputs are heterogeneously regulated.*

Vojnović and *Le Boudec* make the following assumptions :

(A1) Nodes offer to the *EF* aggregate traffic, a service curve β, means that for all t ($t \geq 0$), there exists s, ($s \leq t$) such that

$$A^*(t) \geq A(s) + \beta(t-s)$$

where $A(t)$ denote (*resp.* $A^*(t)$) the input (*resp.* the output) *EF* aggregate data from the node on the interval [0,t].

(A2) The *EF* traffic inputs are mutually independent at network ingress points.

Let A_i ($1 \leq i \leq \mathcal{I}$) be the independent *EF* input traffic.

(A3) Every *EF* input is regulated at the network ingress point. Consequently, for all i, ($1 \leq i \leq \mathcal{I}$), there exists a wide-sense increasing function α_i (called arrival curve) such that :

$$A_i^0(t) - A_i^0(s) \leq \alpha_i(t-s), \ for\ any\ s \leq t$$

where $A_i^0(t)$ represents the data observed on [0,t] of the input traffic A_i at the network ingress.

(A4) $\mathbb{E}[A_i^0(t) - A_i^0(s)] \leq \xi_i(t-s)$, for any $s \leq t$ where $\xi_i = \lim_{t\to\infty} \frac{\alpha_i(t)}{t}$

B. Results of *Vojnović*

Theorem 1 *For a node that offers a super-additive*[1] *service curve β. Then, under (A1)-(A4) and if $\rho < c$, for any t, the upper bound of the probability (denoted $\mathbb{P}$) that the backlog is above a given level b is*

$$\mathbb{P}(Q(t) > b) \leq \mathbb{P}(\tilde{Q}(t) > b) \leq \sum_{k=0}^{K-1} \exp\left(-\frac{2[(b + \beta(s_k) - \rho s_{k+1})^+]^2}{\min\left(\sum_{i=1}^{\mathcal{I}} (\rho_i s_{k+1} + \sigma_i)^2, 4\sum_{i=1}^{\mathcal{I}} \sigma_i^2\right)}\right) \quad (1)$$

for any $K \in \mathbb{N}$, and any $0 = s_0 \leq s_1 \leq \ldots \leq s_K = \tau$.

Theorem 2 *Homogeneous case : Assuming (A1)-(A4) and if $\rho < c$, for any t, the upper bound of the probability (denoted $\mathbb{P}$) that the backlog is above a given level b is*

$$\mathbb{P}(Q(t) > b) \leq \mathbb{P}(\tilde{Q}(t) > b) \leq \sum_{k=0}^{K-1} \exp(-\mathcal{I} g(s_k, s_{k+1}) \quad (2)$$

for any $K \in \mathbb{N}$, and any $0 = s_0 \leq s_1 \leq \ldots \leq s_K = \tau$. where,

- *for, $b > \alpha(v) - \beta(u)$, $g(u,v) = +\infty$*
- *for, $b < \rho v - \beta(u)$, $g(u,v) = 0$*
- *else, $g(u,v) = \frac{\beta(u)+b}{\alpha(v)} \ln \frac{\beta(u)+b}{\rho v} + \left(1 - \frac{\beta(u)+b}{\alpha(v)}\right) \ln \frac{\alpha(v)-\beta(u)-b}{\alpha(v)-\rho v}$*

Corollary 1 *Let a node that offers a service curve $\beta(t) = ct$ and A denote the input aggregate with stationary increments and intensity ρ ($\rho < c$). Then, if a packet arrives in the node at time 0, it holds,*

$$\mathbb{P}_A(Q(0) > b) \leq \frac{c}{\rho} \mathbb{P}(\tilde{Q}(0) > b) \quad (3)$$

Theorem 3 *For a PSRG$(c, 0)$ node and for $u \geq 0$, it is established that, if a node arrives in node at time 0,*

$$\begin{aligned} \mathbb{P}(d(0) > u) &\leq \mathbb{P}_A(Q(0) > cu) \\ &\leq \frac{c}{\rho} \mathbb{P}(\tilde{Q}(0) > cu) \end{aligned} \quad (4)$$

[1] A function, f, is said super-additive if $f(s+t) \geq f(s) + f(t)$ for all $s, t \geq 0$.