Ecole Nationale Supérieure de Mécanique et d'Aérotechnique
Téléport 2 - 1 avenue Clément Ader
BP 40109
86961 Futuroscope Chasseneuil Cedex
Tél : +33 (0)5 49 49 80 80

Title: End-to-end delay of partitioned applications communicating over switched networks

Laboratory: LIAS, ISAE-ENSMA

Keywords: Embedded systems, ARINC 653, end-to-end delay, scheduling, simulation, validation

Problem description:

Avionic embedded network architectures have undergone important evolutions due to the introduction of distributed architectures via the integration of full duplex switched Ethernet technologies. Thus, the avionics functions are distributed on ECUs and communicate between them via the standard ARINC 664p7 protocol. The functions (tasks) executed on the same computer share resources (processor, memory, network, etc.). They are placed in partitions (ARINC 653) to ensure the segregation of functions according to their level of criticality.

The certification of an avionics system relies in particular on the temporal validation of the system. This validation must allow to verify that the temporal constraints (e.g. deadlines) of the tasks are respected and that the end-to-end delays of the messages do not exceed the limits previously set. The complexity of this validation lies in the interdependence of task scheduling on the computers and message transmission over the network.

The validation of ARINC 664p7 has already been the subject of many studies and several approaches (e.g. Forward End-To-End Analysis developed in the laboratory) have already been proposed. There is also a lot of work on single-processor real-time scheduling. However, there is very little work in the literature on real-time scheduling with the specifics of ARINC 653. Thus, the worst-case response times of the tasks on the computers are very strongly overestimated. This leads to an over-dimensioning of the system (both the computer and the network).
The PhD student will start by doing a bibliographic work on the ARINC 653 standard, the AFDX protocol and single-processor real-time scheduling. He or she will have to be autonomous and develop a rigorous work.

The PhD student will then work mainly on the validation of real-time scheduling of tasks in the context of ARINC653. He or she will contribute, for example, to the consideration of partitioning constraints, simple or multi-periodic precedence constraints... In a second time, he or she will integrate the results obtained in the validation process of the worst-case delays of network traversal by the frames. The final objective is to define a tool for the analysis of end-to-end delays, i.e. the delay between the beginning of the execution of a task on a computer and the end of the network crossing of the message it has generated and transmitted.

Prerequisite: Knowledge in real-time scheduling and/or embedded networks is desirable. Good level of English (written and spoken).

Contact: frederic.ridouard@ensma.fr, annie.geniet@univ-poitiers.fr with cover letter, and CV including last known grades and if possible ranking.